Specifications

TFT-LCD module

Model No：AML-FRD500V25103-A

For Customer's Acceptance	
Approved by	**Comment**

	Signature	Date
Prepared by		
Checked by		
Approved by		

Contents

1. Document revision history :

DOCUMENT REVISION	DATE	DESCRIPTION	PREPARED BY	APPROVED BY
A	2017-06-08	First Release.		

2.General Description

AML-FRD500V25103-A is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit a backlight unit, The panel size is 5.0inch and the resolution is 480X854. High image quality a-Si TFT LCD module. Partial-screen display function is available. Sleep and Stand-by modes are available for power saving.

2.1 Features

No	Item	Specification	Remark
1	Display Mode	Normally Black	
2	Screen Size	5.0inch	
3	Resolution	480 × RGB × 854	
4	Color Number	262K	
5	Color Arrangement	Tft Active Matrix	
6	Driver IC	ILI9806E-2C	
7	Back Light	White LED 6*2	
8	Viewing Direction	ALL DIRECTION	
9	Interface	MIPI	
10	Surface Treatment	Uv Cut	
11	touch panel		

2.2 Application

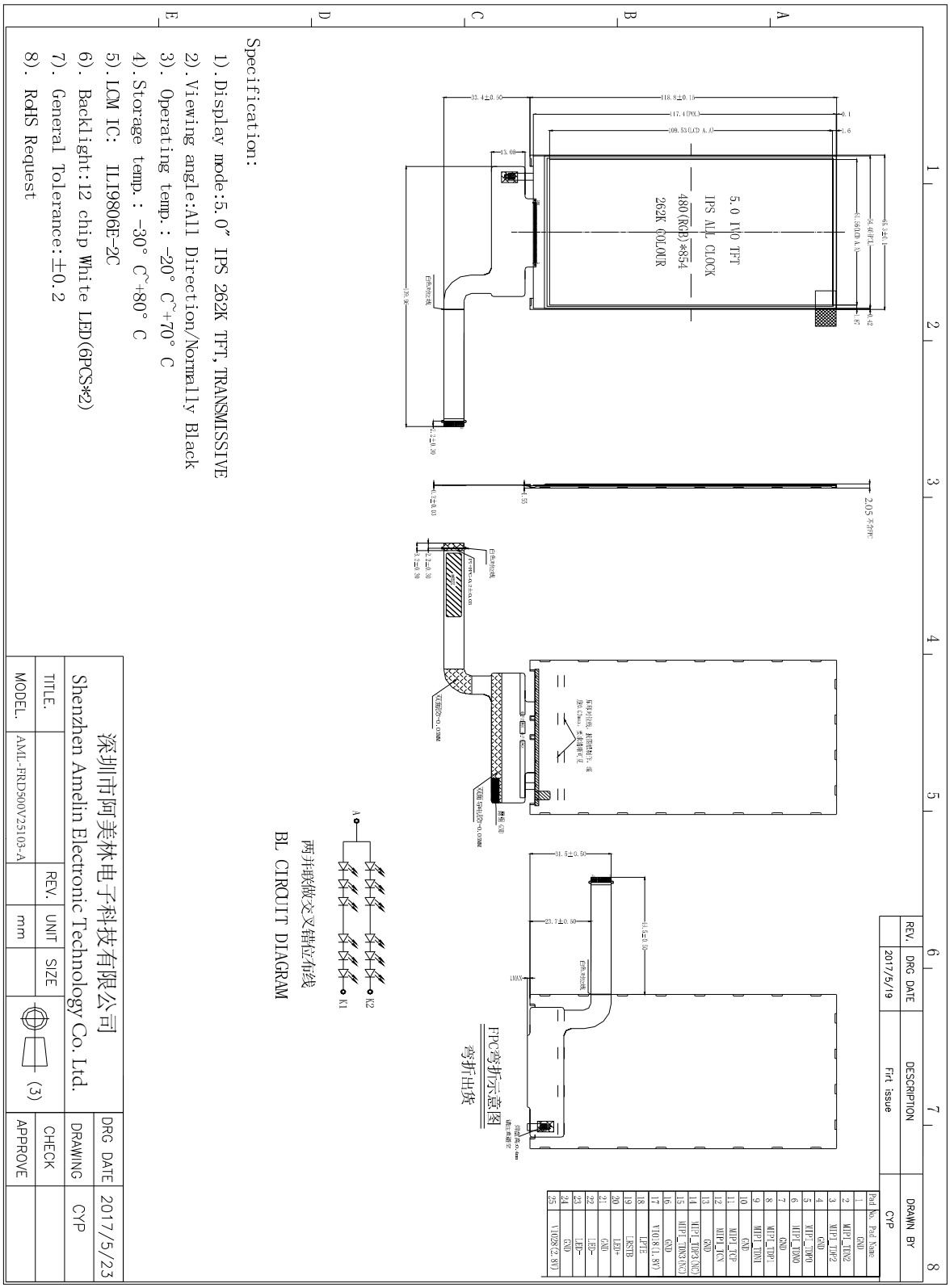
- Mobile phone.
- Portable multimedia device.

3.Outline Dimension

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Parameter	Specifications	Unit
Outline dimensions	65.3(W) ×118.8(H) ×2.05(D) (LCM, not include FPC)	mm
Active area	61.56 (W) ×109.53H)	mm
Resolution	480(H)×RGB× 854(V) dots	-
Dot size	0.08625(H) ×0.08625 (V)	mm

Figure 1: Module specification of the module



4.TFT-LCM Interface Specification

Pin No	Symbol	Description	Note
1	GND	System Ground	
2	**D2N**	No connection	
3	**D2P**	No connection	
4	GND	System Ground	
5	**D0P**	Positive polarity of low voltage differential data 0 signal	
6	**D0N**	Negative polarity of low voltage differential data 0 signal	
7	GND	System Ground	
8	**D1P**	Positive polarity of low voltage differential data 1 signal	
9	**D1N**	Negative polarity of low voltage differential data 1 signal	
10	GND	System Ground	
11	**CLKP**	Positive polarity of low voltage differential clock signal	
12	**CLKN**	Negative polarity of low voltage differential clock signal	
13	GND	System Ground	
14	**D3P**	No connection	
15	**D3N**	No connection	
16	GND	System Ground	
17	IOVCC	Power supply input for I/O: 1.8V	
18	LTE	Tearing Effect Output Signal	
19	RESET	Reset Signal	
20	LEDA	Power supply Anode input for backlight	
21	GND	System Ground	
22-23	LEDK	Power supply Cathode input for backlight	
24	GND	System Ground	
25	VCC	Power supply input for LCM: 2.8V	

5. Absolute Maximum Ratings

5.1 Electrical Maximum Ratings – for IC Only

Table 3: Electrical Maximum Ratings – for IC

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage (VCC)	VCC	-0.3	+4.0	V	1
Power supply voltage (IOVCC)	IOVCC	-0.3	+3.6	V	1

Note:

1.IOVCC,VCC, GND must be maintained.

2.The modules may be destroyed if they are used beyond the absolute maximum ratings.

5.2 Environmental Condition

Table 4

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature	-20℃	+70℃	-30℃	+80℃	Dry
Humidity (Note 1)	80% max. RH for Ta 40℃< 50% RH for 40℃ < Ta Maximum operating temperature				No condensation

Note 1: Product cannot sustain at extreme storage conditions for long time.

6. Electrical Specifications

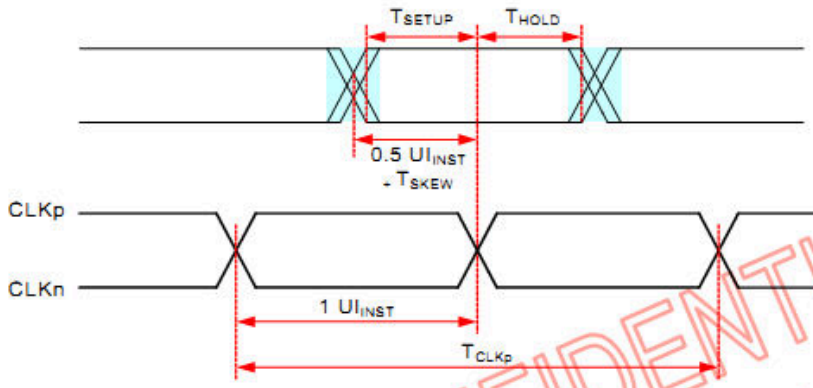
Typical Electrical Characteristics

At Ta = 25 ℃, VCC = 2.6V to 3.3V, IOVCC= 1.65V to 3.3V GND=0V.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (analog)	VCC-GND		2.6	2.8	3.3	V
Supply voltage (logic)	IOVDD-GND		1.65	1.8	3.3	V
Supply current (Logic & LCD)	ICC	VCC=2.8V	-	-	50	mA
Supply voltage of white LED backlight	VLED =$V_{(BL+)}$-$V_{(BL-)}$	Forward current =40 mA Number of LED dies = 12	18	19.2	20.4	V
Luminance (on the module surface)			-	250	-	cd/m^2

7.Timing Characteristics

High Speed Data Transmission: Data-Clock Timing



Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	1		12.5	ns	1,2,10
Data to Clock Skew [measured at transmitter]	T_{SKEW}[TX]	-0.15		0.15	UI_{INST}	3
		-0.2		0.2	UI_{INST}	4
Data to Clock Setup Time [measured at receiver]	T_{SETUP}[RX]	-0.15		0.15	UI_{INST}	5
		-0.2		0.2	UI_{INST}	6
Data to Clock Hold Time [measured at reciever]	T_{HOLD}[RX]	-0.15		0.15	UI_{INST}	5
		-0.2		0.2	UI_{INST}	6
20% - 80% rise time and fall time	t_R / t_F	100			ps	9
				0.3	UI_{INST}	7
				0.35	UI_{INST}	8

Note:

1. This value corresponds to a minimum 80 MHz data rate.

2. The minimum UI shall not be violated for any single bit period, i.e.,any DDR half cycle within a data burst.

3. Total silicon and package delay budget of 0.3 UIINST when D-PHY is supporting maximum data rate = 1Gbps.*

4. Total silicon and package delay budget of 0.4 UIINST when D-PHY is supporting maximum data rate > 1Gbps.*

5. Total setup and hole window for receiver of 0.3 UIINST when D-PHY is supporting maximum data rate = 1Gbps.*

6. Total setup and hole window for receiver of 0.4 UIINST when D-PHY is supporting maximum data rate > 1Gbps.*

7. Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).

8. Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

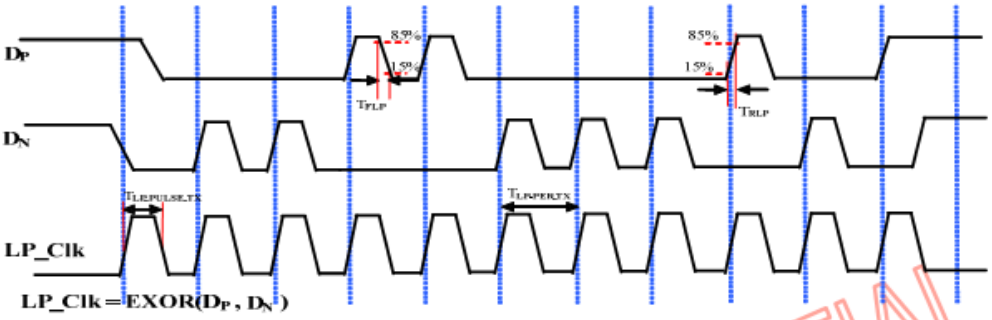
9. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.

10. For MIPI speed limitation:

[1] Per lane bandwidth is 1Gbps,

[2] Total Bit Rate: 4Gbps for 8-8-8; 3Gbps for 6-6-6; and 2.67Gbps for5-6-5.

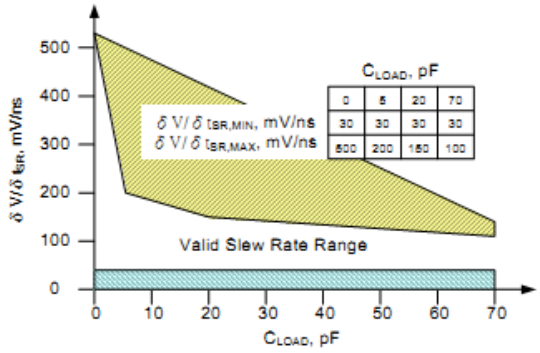
LP Transmission AC Specification



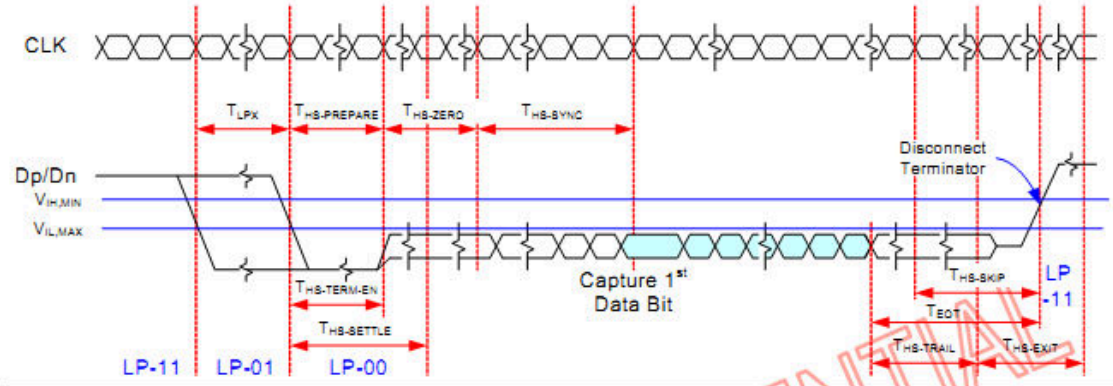
Parameter		Symbol	Min	Typ	Max	Units	Notes
15%-85% rise time and fall time		T_{RLP} / T_{FLP}			25	ns	1
30%-85% rise time and fall time		T_{REOT}			35	ns	1,5,6
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after STOP state or last pulse before stop state	$T_{LP-PULSE-TX}$	40			ns	4
	All other pulses		20			ns	4
Period of the LP exclusive-OR clock		$T_{LP-PER-TX}$	90			ns	
Slew Rate@ C_{LOAD} = 0pF		$\delta V/\delta t_{SR}$	30		500	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 5pF			30		200	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 20pF			30		150	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 70pF			30		100	mV/ns	1,2,3,7
Load Capacitance		C_{LOAD}			70	pF	1

Note:

1. *CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.*
2. *When the output voltage is between 15% and below 85% of the fully settled LP signal levels.*
3. *Measured as average across any 50 mV segment of the output signal transition.*
4. *This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.*
5. *The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.*
6. *With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the Lane.*
7. *This value represents a corner point in a piecewise linear curve as bellowed.*



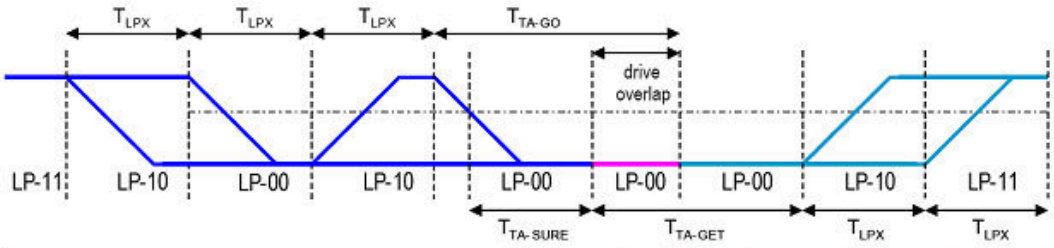
High-Speed Data Transmission in Bursts



Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Note:
1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.
3. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Turnaround Procedure



Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	50		75	ns
Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5T_{LPX}$		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		$4T_{LPX}$		ns

8.Power Supply Configuration

19.4.1. Power Structure

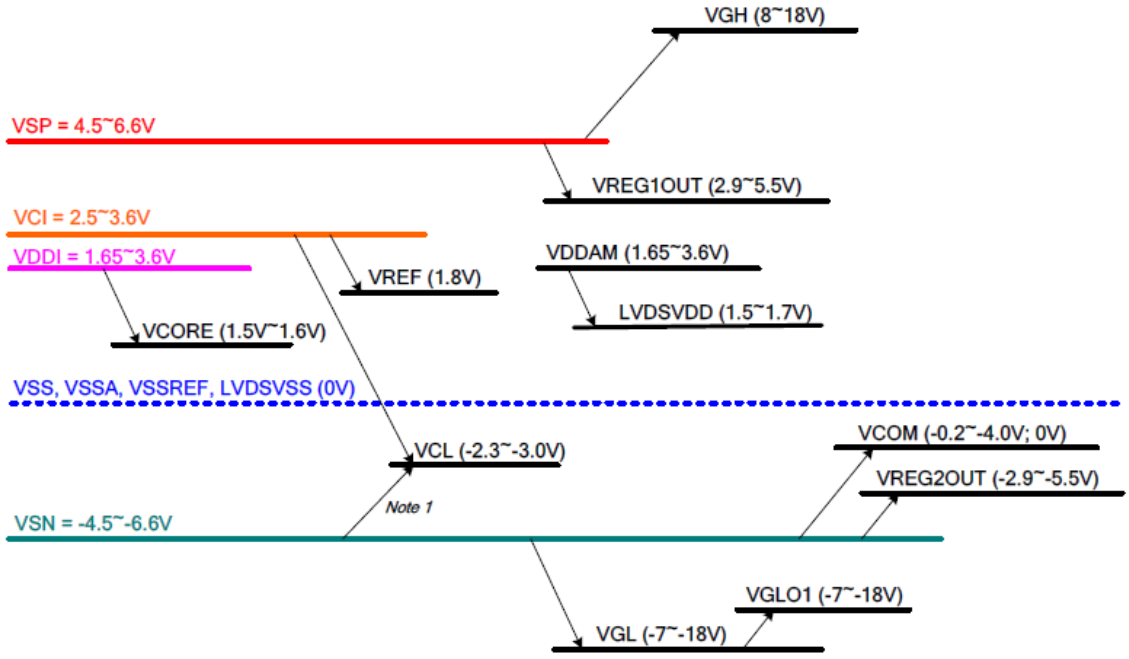


Figure 130: Power Structure of Power Mode 4

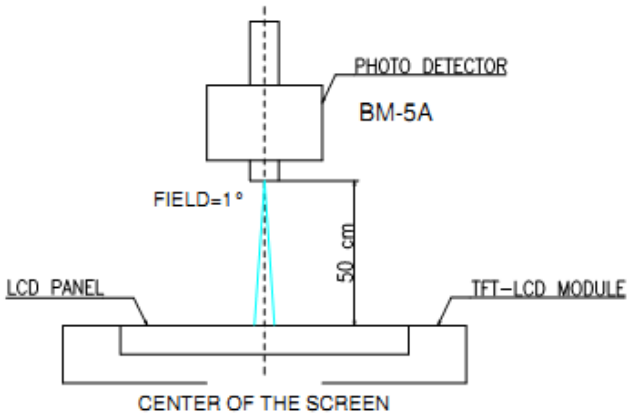
9.Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time	Rise	Tr	θ=0°	--	20	35	ms	Note 3
	Fall	Tf		--	15	35	ms	
Contrast ratio		CR	At optimized viewing angle	800	1000	--		Note 4
NTSC		%	θ=0°	--	70	--		
Viewing Angle	Top		CR 100		80		deg.	Note 5
	Bottom				80			
	Left				80			
	Right				80			
Transmittance		%			3.72%			
Chromaticity	White	X	θ=0°	0.284	0.314	0.344		Based on H466 BLU spectrum.
		Y	θ=0°	0.321	0.351	0.381		
	Red	X	θ=0°	0.620	0.650	0.680		
		Y	θ=0°	0.307	0.337	0.367		
	Green	X	θ=0°	0.202	0.232	0.262		
		Y	θ=0°	0.544	0.574	0.604		
	Blue	X	θ=0°	0.110	0.140	0.170		
		Y	θ=0°	0.094	0.124	0.154		

Note 1: Measured under Ambient temperature =25℃±2℃.

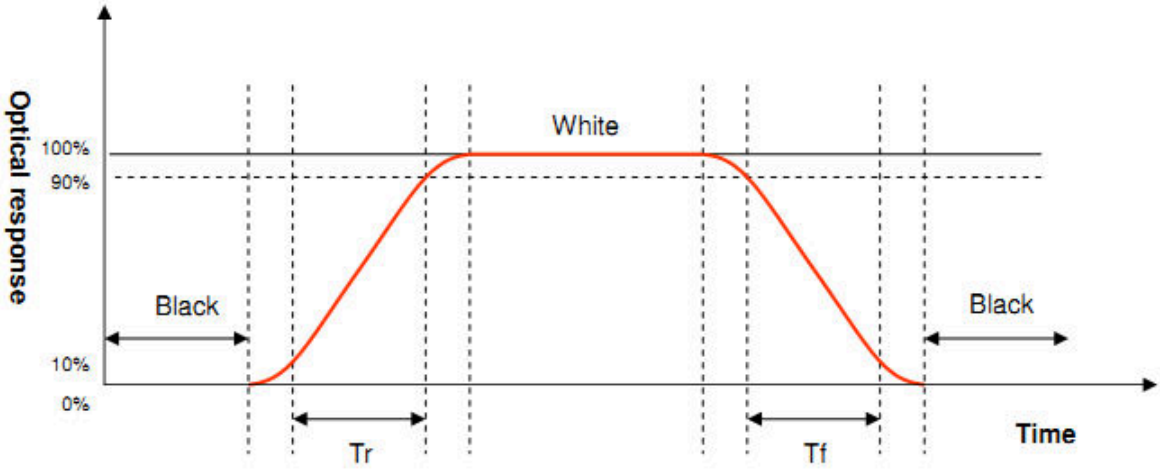
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

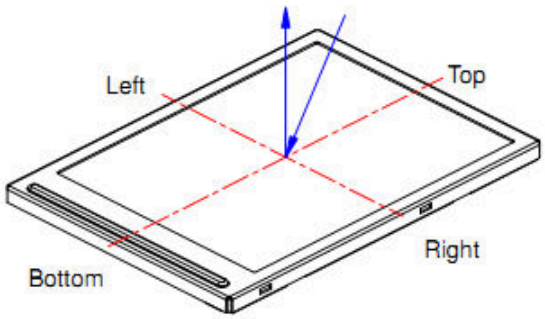


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.

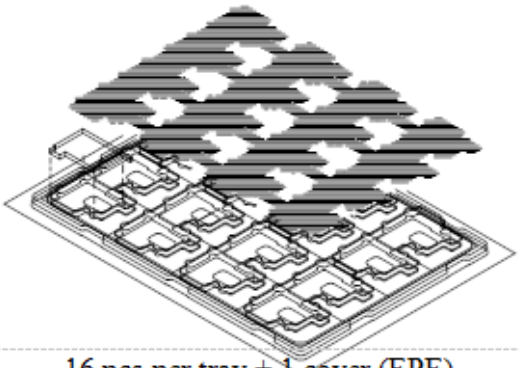
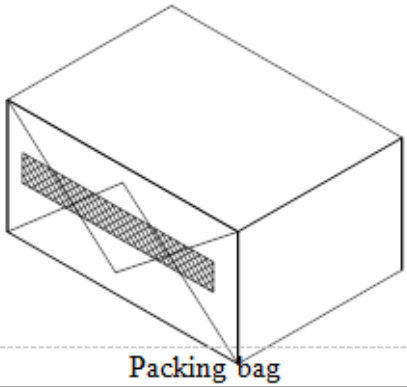
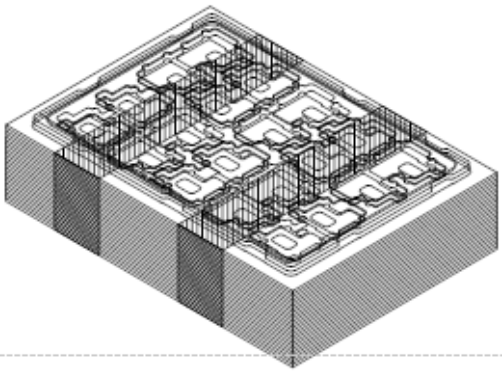
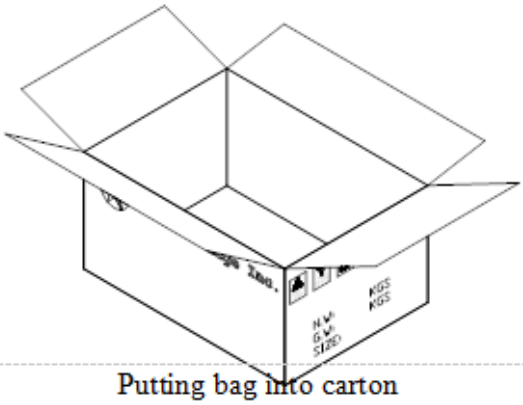
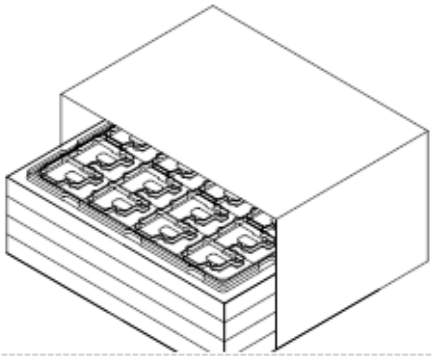
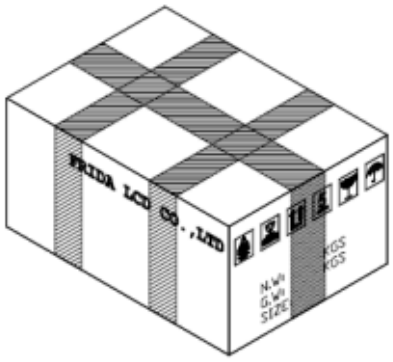


Note 6: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

10.Reliability Test Items

Item	Test Condition		Criterion
High Temperature Storage	80 ℃, 120 hrs		There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.
Low Temperature Storage	-30 ℃, 120 hrs		
High Temp. & High Humidity Storage	40 ℃, 80％ RH, 120 hrs		
Vibration Test (Non-operating)	Freq.:10~55~10 Hz, Amp.:1.5mm 1 hr for each direction of X, Y, Z		
Electrostatic Discharge Test (Non-operating)	Terminals	150 pF, 0 Ω, ±300 V, Contact	
	Panel	150 pF, 330 Ω, ±8 KV, Air	
Thermal Shock (Static)	-30℃, 30 min /70℃, 30 min, 20 cycles		
High Temperature Operation	70 ℃, 120 hrs		
Low temperature Operation	-20 ℃, 120 hrs		
High Temperature & High Humidity (Operating)	40 ℃, 70％ RH, 120 hrs		
FPC Peeling Strength Test	Pull speed: 50 mm/min, +90°,		> 400gf/cm

11. Package

1  16 pcs per tray + 1 cover (EPE)	4  Packing bag
2  25 trays + 1 dummy tray = 400 ps	5  Putting bag into carton Protected by 6 pieces of cushion EPE sheet
3  Putting trays into anti-electrostatic bag	6 

12.Precautions

Please pay attentions to the followings as using the LCD module.

Handling

(a) Do not apply strong mechanical stress like drop, shock or any force to LCD module. It may cause improper operation, even damage.

(b) Because the polarizer is very fragile and easy to be damaged, do not hit, press or rub the display surface with hard materials.

(c) Do not put heavy or hard material on the display surface, and do not stack LCD modules.

(d) If the display surface is dirty, please wipe the surface softly with cotton swab or clean cloth.

(e) Avoid using Ketone type materials (e.g. Acetone), Toluene, Ethyl acid or Methyl chloride to clean the display surface. It might damage the touch panel surface permanently. The recommended solvents are water and Isopropyl alcohol.

(f) Wipe off water droplets or oil immediately.

(g) Protect the LCD module from ESD. It will damage the LSI and the electronic circuit.

(h) Do not touch the output pins directly with bare hands.

(i) Do not disassemble the LCD module.

(j) Do not lift the FPC of Touch Panel.

Storage

(a) Do not leave the LCD modules in high temperature, especially in high humidity for a long time.

(b) Do not expose the LCD modules to sunlight directly.

(c) The liquid crystal is deteriorated by ultraviolet. Do not leave it in strong ultraviolet ray for a long time.

(d) Avoid condensation of water. It may cause improper operation.

(e) Please stack only up to the number stated on carton box for storage and transportation. Excessive weight will cause deformation and damage of carton box.

Operation

(a) When mounting or dismounting the LCD modules, turn the power off.

(b) Protect the LCD modules from electric shock.

(c) The Driver IC control algorithms stated above should always obeyed to avoid damaging the LSI and electronic circuit.

(d) Be careful to avoid mixing up the polarity of power supply for backlight.

(e) Absolute maximum rating specified above has to be always kept in any case. Exceeding it may cause non-recoverable damage of electronic components or, nevertheless, burning.

(f) When a static image is displayed for a long time, remnant image is likely to occur.

(g) Be sure to avoid bending the FPC to an acute shape, it might break FPC.

(h) Most of the touch screens have air vent to equalize the inside air pressure to the outside one. The air vent must be open and liquid contact must be avoided as the liquid may be absorbed if the liquid is accumulated near the air vent.

(i) For the fragility of ITO film, it should avoid to use too tapering pen as the input material.

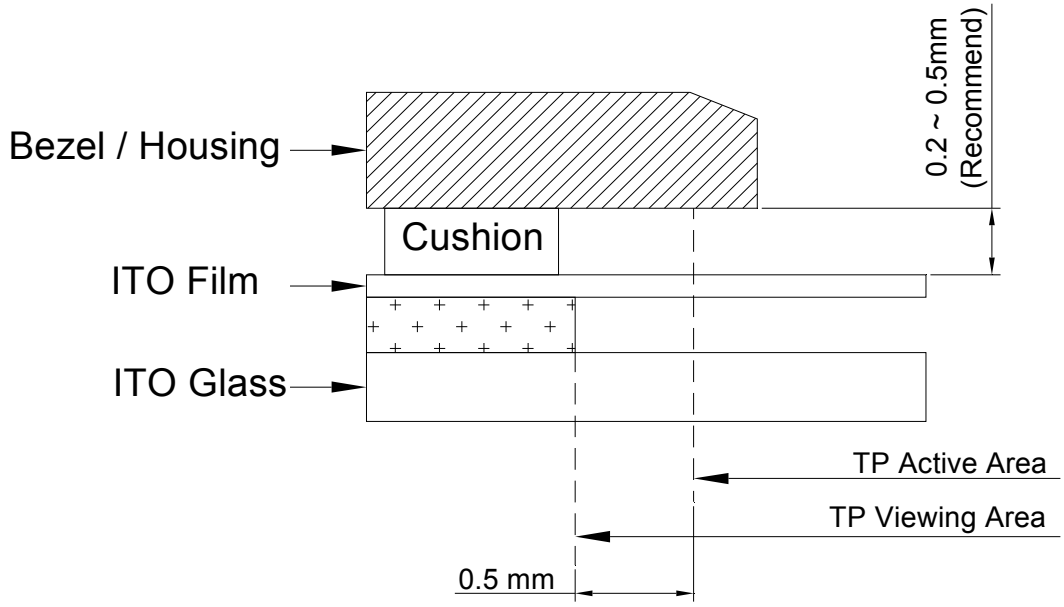
Touch Panel Mounting Notes

(a) If a cushion is used between bezel/housing and film must be choose as free as enough to absorb the expansion and contraction to avoid the distortion of film.

(b) The cushion must be placed out of the Viewing Area.

(c) Bezel/Housing edge must be posited between Key Area and Viewing Area. The edge enters the Key Area may cause unexpected input if the gap is too narrow or foreign particles like dusts exist between Bezel/Housing and ITO film.

(d) Mounting example:



The corner part has conductivity. Do not touch any metal part after mounting.

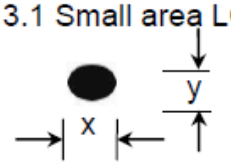
Others

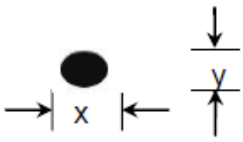
a) If the liquid crystal leaks from the panel, it should be kept away from the eyes or mouth.

b) For the fragility of polarizer, it is recommended to attach a transparent protective plate over the display surface.

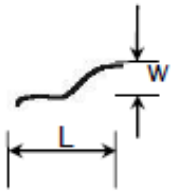
c) It is recommended to peel off the protection film on the polarizer slowly so that the electrostatic charge can be minimized.

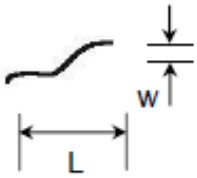
13. Inspection standard

<table>
<tr><th>No</th><th>Item</th><th>Criterion</th><th></th></tr>
<tr><td>01</td><td>Outline Dimension</td><td>In accord with drawing</td><td></td></tr>
<tr><td>02</td><td>Position-finding Dimension Assemble Dimension</td><td>In accord with drawing</td><td></td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD black spots, white spots (Round type)</td><td>Round type: non display
3.1 Small area LCD
Unit : mm
 

<table><tr><th>Dimension</th><th>Qualified Quantity</th></tr><tr><td>D≤0.1</td><td>Ignore</td></tr><tr><td>0.1<D≤0.15</td><td>2</td></tr><tr><td>D>0.15</td><td>0</td></tr></table></td><td></td></tr>
<tr><td>3.2Large area LCD
 

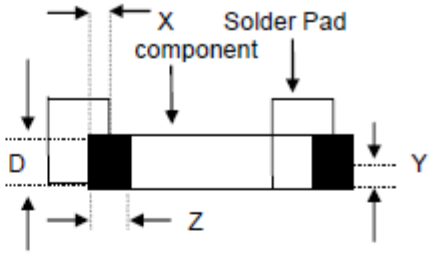
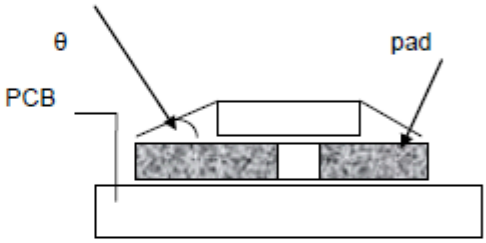
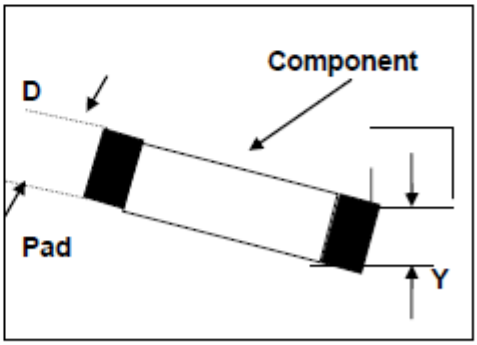
<table><tr><th>Dimension</th><th>Qualified Quantity</th></tr><tr><td>D≤0.1</td><td>Ignore</td></tr><tr><td>0.1<D≤0.15</td><td>2</td></tr><tr><td>0.15<D≤0.20</td><td>1</td></tr><tr><td>D>0.20</td><td>0</td></tr></table>C-STN : if D>0.1 , unqualified</td><td></td></tr>
</table>

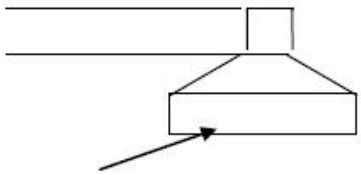
<table>
<tr><td rowspan="2">04</td><td rowspan="2">LCD black spots, white spots (Line Style)</td><td>4.1 Small area LCD
Unit : mm
 

<table><tr><th>Length</th><th>Width</th><th>Qualified Quantity</th></tr><tr><td>-</td><td>≤0.015</td><td>Ignore</td></tr><tr><td>≤1.0</td><td rowspan="2">0.015<W≤ 0.025</td><td>2</td></tr><tr><td>≤2.0</td><td>1</td></tr><tr><td>≤1.0</td><td>0.025<W≤ 0.05</td><td>1</td></tr><tr><td>-</td><td>D>0.05</td><td>According to circle</td></tr></table></td><td></td></tr>
<tr><td>4.2Large area LCD
 

<table><tr><th>Length</th><th>Width</th><th>Qualified Quantity</th></tr><tr><td>-</td><td>≤0.015</td><td>Ignore</td></tr><tr><td>≤2.0</td><td>0.015<W≤ 0.025</td><td>2</td></tr><tr><td>≤1.0</td><td>0.025<W≤ 0.05</td><td>1</td></tr><tr><td>-</td><td>D>0.05</td><td>According to circle</td></tr></table>CSTN : If W ⩾ 0.015 , unqualified
Ignore beyond viewing area</td><td></td></tr>
<tr><td>05</td><td>LCD Scratch 、Threadlike Fiber</td><td>Same to NO.3 circle
sightline and surface of LCD is vertical
(2)Same to NO.3 line style</td><td></td></tr>
<tr><td>06</td><td>POL</td><td>It is not admissible that POL is beyond the edge of glass, else, unqualified.
It is essential that POL is over the 50 percent of width of frame , else ,unqualified.
According to the drawing in case of special definition.</td><td></td></tr>
<tr><td>07</td><td>IC/FPC Bonding</td><td>Scratch</td><td>Reject</td><td></td></tr>
</table>

		Intensity Of Adhesion	If lower than specification, reject	
		Gold Fold Twist	Reject	
07	IC/FPC Bonding	Silicon	According to outline, no gold outside, seal can not be higher than LCD	
		FPC Gold Sever	Reject	
08	SMT	Lack of Component、Polarity Inverse	If exist, reject	
		Leak Solder、Virtual Solder	If exist, reject	
		Short Circuit In Solder Point	If exist, reject	
		Tin Ball	If exist, reject	
		Tin Acumination	If visual, reject	
		Height Solder Point	If higher 0.5mm than component. reject	
		Height of component	Either side higher 0.5mm than component, reject	

		Component Shift	 X<3/4Z reject y>1/3D reject	
08	SMT	Few Tin	 If θ≤20° reject	
		Component Deflection	 If Y>1/3D reject	
		Component Carcass Sideways	Reject	

		Component Carcass Sideways	If exist with visual inspection , reject	
		Lot Tin	A: Tin accrete the solder side completely , hollowly ,Ok B: Tin accrete the solder side completely , full circle arc , ok C: Jointing include whole solder side, height of tin>50 percent of height of component, reject	
		Few Tin	A: Tin accrete the solder side completely , hollowly ,Ok B: height of tin > 1/3 of solder side of component , ok C: height of tin ≤ 1/3 of solder side of component, reject	
08	SMT	Normal  Jointing side		
09	Light	Short circuit 、 Open circuit	Forbid	
		Quality of CSTN Display	1、Rolling strake with visual inspection, forbid 2、Differentness of color in viewing area with visual inspection (full white、red、green、blue), forbid 3 、 Display change with visual inspection , forbid	